

40 $\mu\text{m}^2$  Ae NPN  
Vce=7 to 16V, 1V step

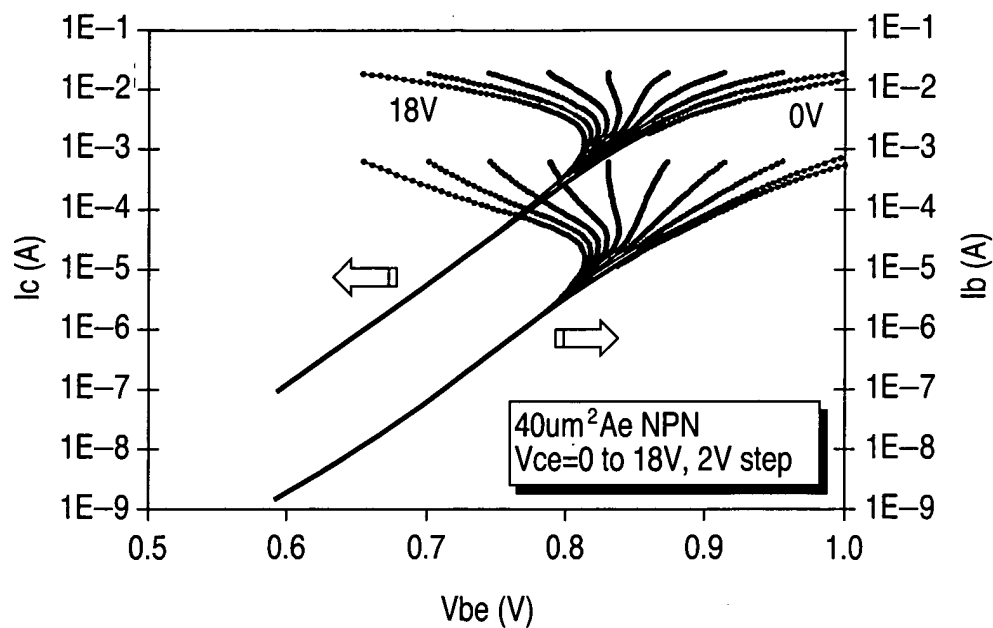
Beta ( )

16V 7V  
Vce

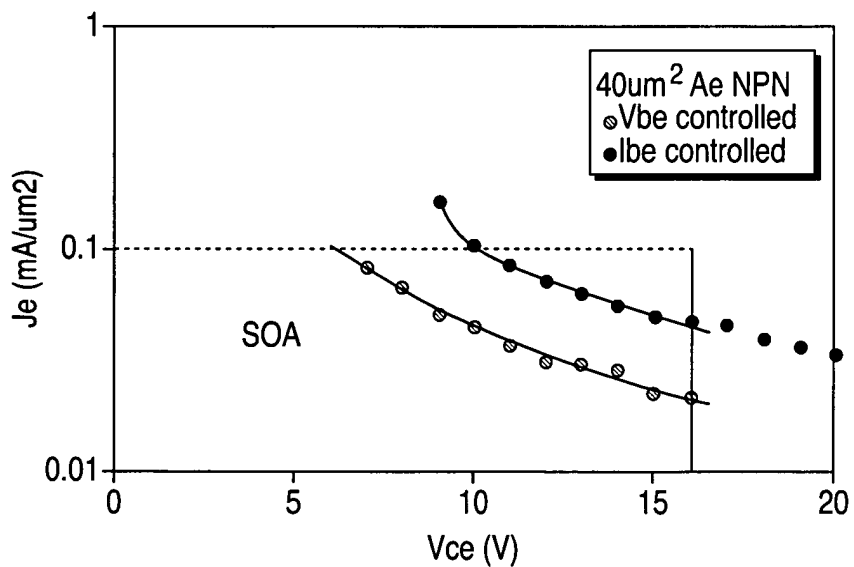
Vbe (V)

METHOD FOR QUANTIFYING SAFE OPERATING AREA FOR BIPOLAR  
JUNCTION TRANSISTOR

Inventor: Kim et al.  
Application No. 10/688,550



**FIG. 2B**  
(PRIOR ART)



**FIG. 3**  
(PRIOR ART)

METHOD FOR QUANTIFYING SAFE OPERATING AREA FOR BIPOLAR  
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Application No. 10/688,550

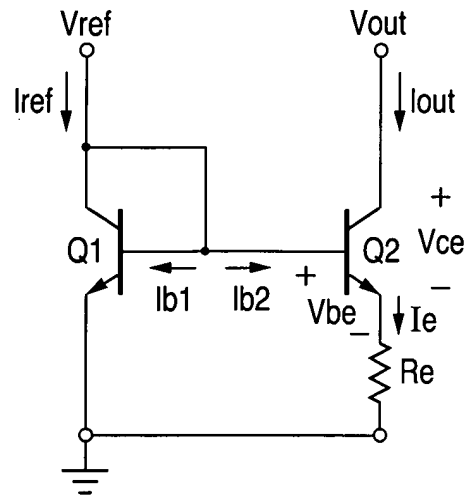


FIG. 4

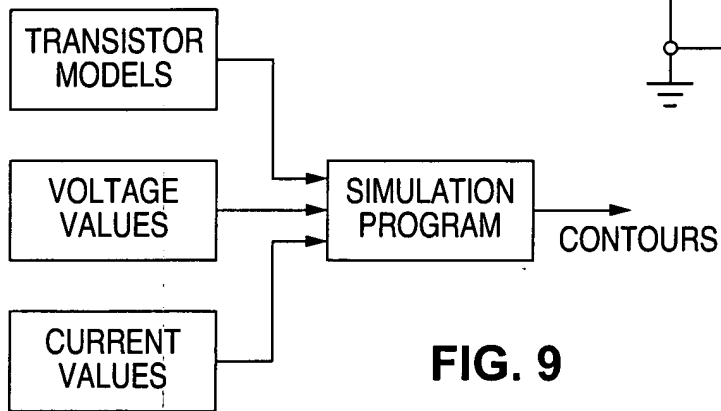


FIG. 9

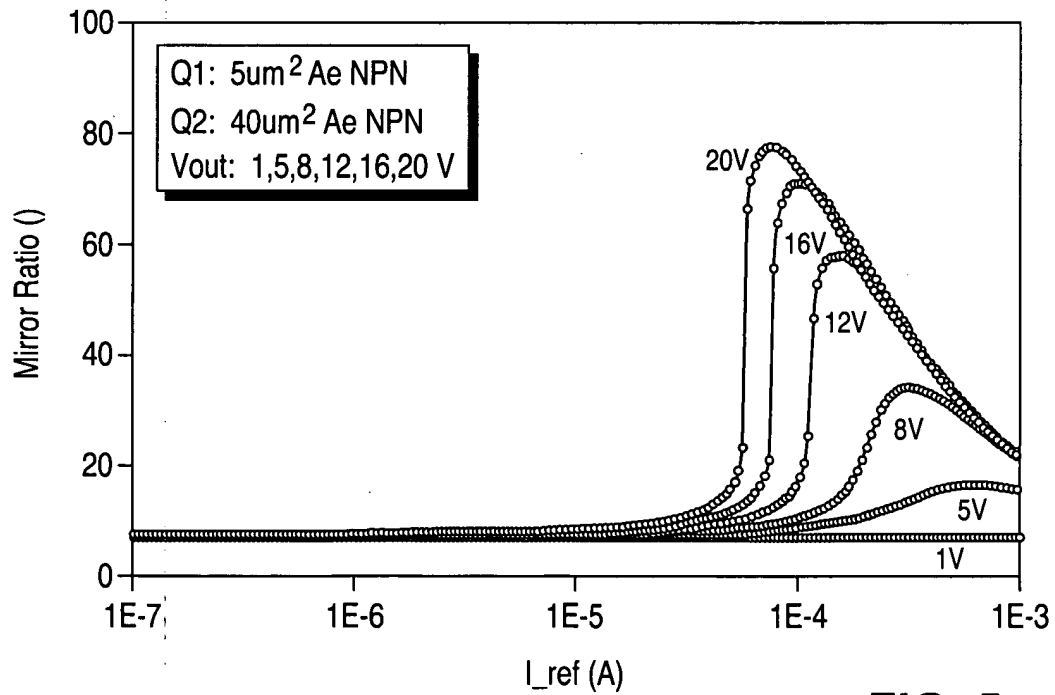


FIG. 5

METHOD FOR QUANTIFYING SAFE OPERATING AREA FOR BIPOLAR  
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Application No. 10/688,550

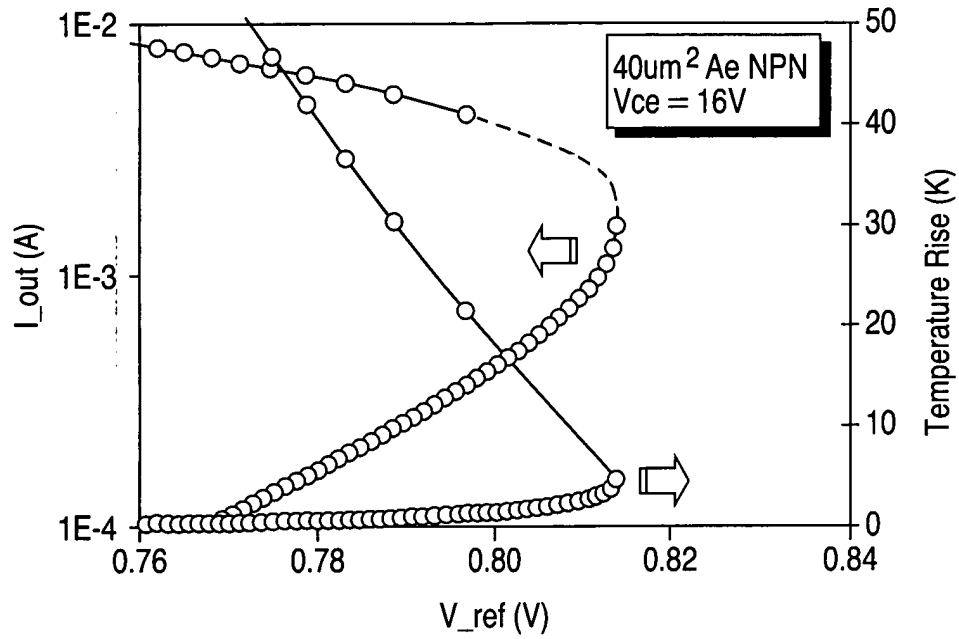


FIG. 6

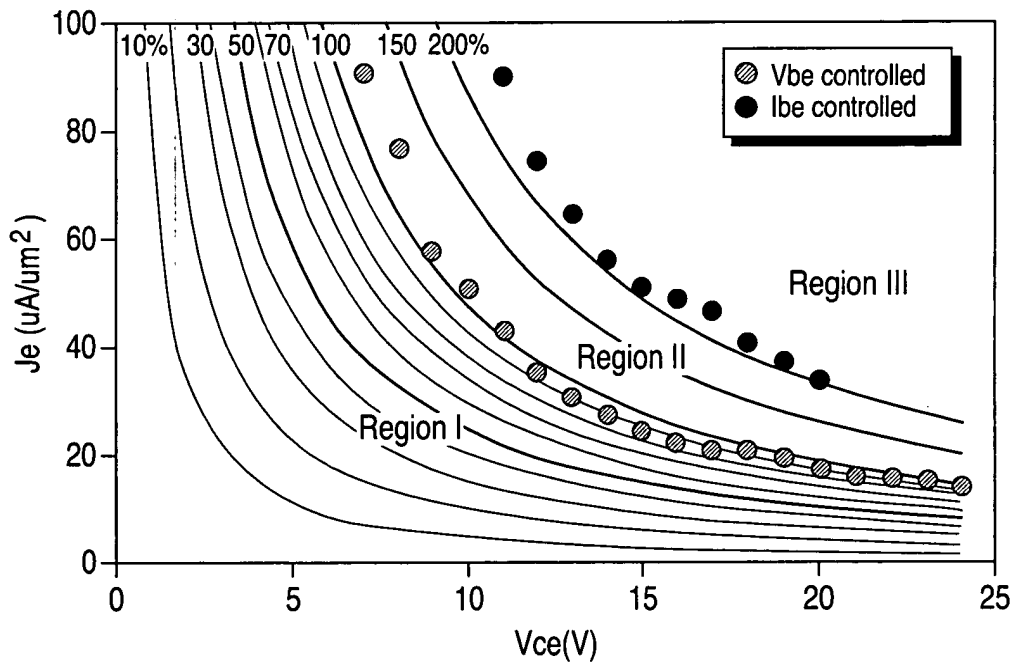


FIG. 8

# METHOD FOR QUANTIFYING SAFE OPERATING AREA FOR BIPOLAR JUNCTION TRANSISTOR

Inventor: Kim et al.

Application No.: 10/688,550

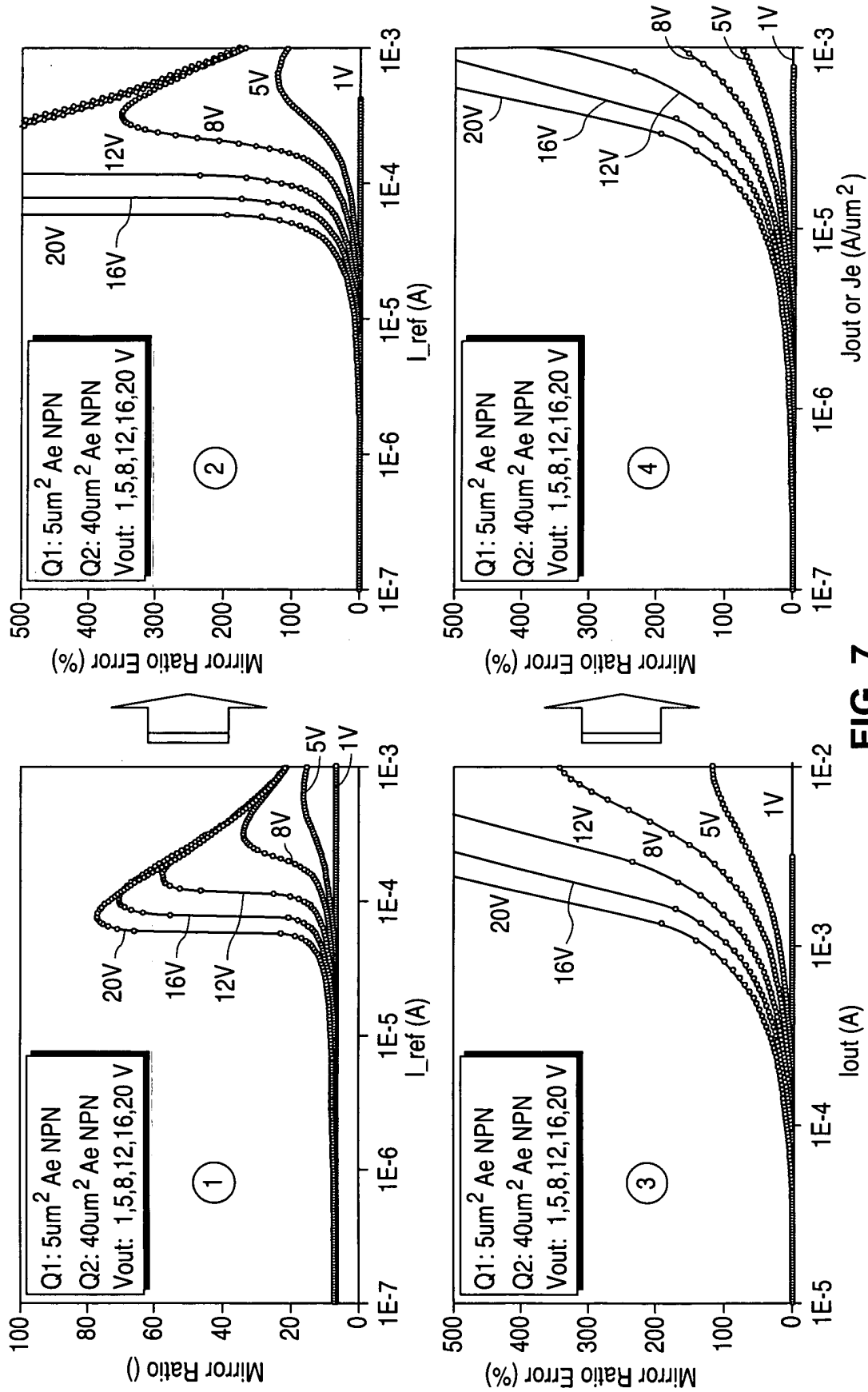


FIG. 7